BIMA
Technical Memo #71

A New Correlator Architecture Eases Wiring Problem

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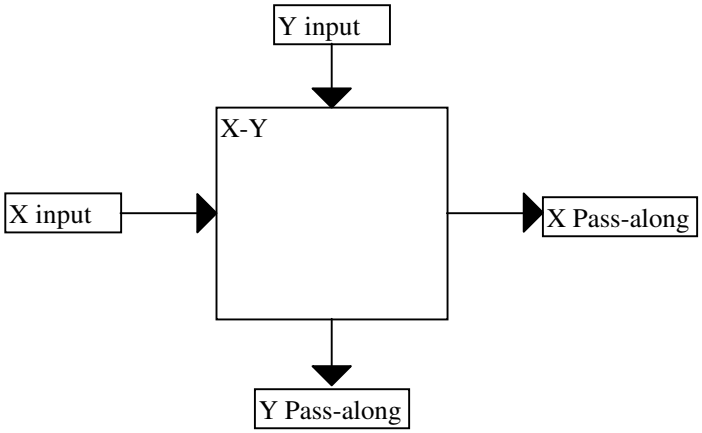
Abstract

A big problem in correlator design is the large number of signal wires that must be distributed to the correlators. A 10 antenna system has 45 baselines. Each antenna must supply signal to 9 correlators for a total of 90 signal paths. If each antenna has a single digital sampler that samples to two bits then there are 180 signal pairs that must be carefully designed to arrive at the proper place at exactly the correct time. If an extra antenna is added there are 220 signal pairs to deal with and the whole signal distribution system must be redesigned. By a simple strategy it is possible to limit the signal paths from each antenna to two. It is also possible to expand the system indefinitely without the need to redesign the distribution of signals.

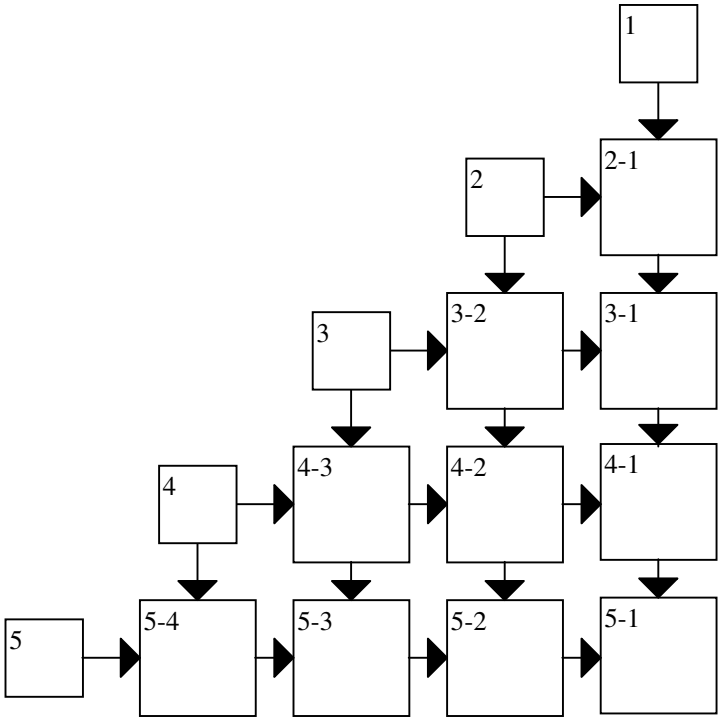
Discussion

Schemes have been presented that attempt to solve the distribution problem by putting the signals on a bus. A bus structure suffers from many problems. Each signal line acts like a transmission line with stubs located at each point that a card taps onto it. Due to the finite speed of light, the signal cannot arrive at all of the cards at once. If a card is taken out of the system, the bus will change it's characteristics potentially causing problems for the other cards on the bus. The cards must be designed with signal receivers that have high input impedance and the path length on the card from the bus to the receiver must be kept as short as possible. In contrast to the bus architecture, a scheme that uses properly terminated individual transmission lines is simple to design and control. The receiver or the line driver may be located anywhere on the card as long as the cable impedance, the connector impedance and the board trace impedance are all the same. If a card is removed from such a system it cannot affect any of the other cards. The length of individual transmission lines can be carefully controlled so that the signals all arrive at the same time. A system built of individual transmission lines holds the promise of the greatest bandwidth.

A simplification in signal distribution will result if each correlator stores each of it's input signals in a buffer that delays it by one system clock tick causing it to be re-synchronized to the system. A line driver from each buffer is used to pass the signal on to the next correlator input.



Single Correlator Element
Each pass-along is delayed by one clock tick.



Array of Five Antennas and Ten Baselines

The correlators are arranged in an array in such a way that the X and Y signals to any correlator in the array are delayed by the same amount. As seen above, antenna 5 and antenna 1 are both delayed by three clock ticks before they reach baseline 5-1. The basic principal involved here is the fact that the correlation function will not change if the things being correlated are equally delayed. This interconnection scheme has the added benefit that no added signal distribution is required if the array is expanded at some future date.

There is a widely held myth that, because of the speed of light, a machine must be made physically small in order to make it as fast as possible. The imagined requirement for small size leads to cooling problems since electronics tends to dissipate more power as it is driven to higher speeds. More power dissipated in a smaller space can make the equipment very warm. Fortunately, small physical size is not usually required. In the above scheme equal delays were added to both inputs of a correlator with no adverse effect on the data rate. In general, adding delays to the inputs of any arithmetic element will not affect the data rate. In situations where the next calculation is dependent upon the last result, time delay due to path length can result in data rate problems. There is nothing in the design of a correlator that requires a trade-off between size and speed. As long as careful attention is paid to the lengths of the signal and clock lines interconnecting the system elements, there will be no sacrifice in speed due to large size.